ABSTRACT OF THE DISCLOSURE

A processor comprising a new architectural feature called a Backing Register File, where a Backing Register File is a set of randomly accessible registers capable of holding values, and further are directly connected to the processor's register files. The processor's register files are in turn connected to the processor's execution units. A Backing Register File is visible and controllable by users, allowing them to make use of a larger local address space increasing execution unit throughput thereby, while not changing the size of the register files themselves.